# Lab 4: Design an Electronic Lock

(2+2+2 hours)

## Goal

To learn how to implement an Electronic Lock by using FSM. .

## Procedure

Implement the Electronic lock learnt in class with the following function diagram (see slides of lecture 5).



1. Draw the state diagram of the FSM in the above figure. 画状态图
2. Write the behavior level Verilog module of the FSM. 写状态机代码
3. Write a testbench to simulate the FSM by using the method in Lab 3. 仿真状态机
4. Write the Verilog description of the whole design in the above figure and test it in your Basys3 board. 写全部代码
5. Synthesis the FSM by hand to draw the circuit of the FSM with only the D flipflops and AND/OR/NOT gate. Verify the circuit you synthesized and the circuit synthesized by Vivado.用d触发器和与或非门画状态机电路，和vivado对比
6. From the synthesized circuit by your own, write the Verilog module of the FSM: For the next-state logic and the output logic, use “assign” statement to describe the combinational logic, and for the D flipflop, use “always” statement to describe it.用自己写的电路来写状态机代码，次态逻辑和输出用assign，d触发器用always
7. For the whole design, replace the FSM module designed in step 2) with that designed in step 6), and implement the whole design in your board. 用6代替2，写完全部代码